CST-101 (Digital Logic I)

(Major Core)

Course code number	CST- 101	**Course Title**	Digital Logic I
Semester hours	**4 hours**	**No. of Credit Units**	**3**
Prerequisite	**-**	**Course Coordinator**	

Course Description

This course introduces students to the basic concepts of digital systems, including analysis and design. Combinational logic will be covered. Students will gain experience with several levels of digital systems, from simple logic circuits to hardware description language.

Course Objectives

- Apply Boolean algebra and other techniques to express and simplify logic expressions.
- Analyze and design combinational digital systems.
- Use different techniques such as hardware description languages and functional programming languages to design digital systems.

Learning Outcomes

The main learning objective of this class is to have a strong knowledge of Digital Electronics. This includes the functionality of logic gates, simplifying digital circuits, Boolean expression, combinational and sequential circuits. The course is designed to provide a hand-on approach to the concepts taught in the class.

Assessment Plan for the Course

Paper Exam: 60%

Attendance: 10%

Test/ Quiz: 10%

Lab: 10%

Lab Assessment: 10%

Tentative Lecture Plan

CST-101 : Digital Logic I **Third Semester**

Text Book : Digital Fundamentals (11th Edition)
by Thomas L. Floyd

Period : 45 periods for 15 weeks (3 periods/week) (Lecture + Lab)

No.	Chapter	Page	Period	Detail Lecture Plan
	Chapter 1 Introductory Concepts	15-25	**2**	
1.	1-1 Digital and Analog Quantities 1-2 Binary Digits, Logic Levels, and Digital Waveforms	16-19 19-25	2	E.g. 1-1, 1-2 Problem: 1 to 14
	Chapter 2 Number Systems, Operations, and Codes	65-109	**5**	
2.	2-1 Decimal Numbers 2-2 Binary Numbers 2-3 Decimal-to-Binary Conversion 2-4 Binary Arithmetic	66-67 67-70 71-73 74-77	1	E.g. 2-1 to 2-11 Problem: 1 to 18
3.	2-5 Complements of Binary Numbers 2-6 Signed Numbers	77-79 79-84	2	E.g. 2-12 to 2-18 Problem: 19 to 30
4.	2-8 Hexadecimal Numbers 2-9 Octal Numbers 2-10 Binary Coded Decimal (BCD) 2-11 Digital Codes	92-98 98-100 100-103 104-109	2	E.g. 2-24 to 2-38 Problem: 37 to 62
	Chapter 3 Logic Gates	125-153	**4**	
5.	3-1 The Inverter 3-2 The AND Gate 3-3 The OR Gate	126-129 129-135 136-140	1	E.g. 3-1 to 3-5, 3-7 to 3-9 Problem: 1 to 16
6.	3-4 The NAND Gate 3-5 The NOR Gate	140-145 145-149	2	E.g. 3-10 to 3-19 Problem: 17 to 24
7.	3-6 The Exclusive-OR and Exclusive-NOR Gates	149-153	1	E.g. 3-20, 3-21 Problem: 25 to 28
8.	**Multisim Lab 1**		**1**	Introduction to Multisim Simulation on logic gates
9.	**Multisim Lab 2**		**1**	E.g. 3-6

No.	Chapter	Page	Period	Detail Lecture Plan
	Chapter 4 Boolean Algebra and Logic Simplification	191-232	**8**	
10.	4-1 Boolean Operations and Expressions 4-2 Laws and Rules of Boolean Algebra	192-193 193-199	2	E.g. 4-1, 4-2 Problem: 1 to 8
11.	4-3 DeMorgan's Theorems 4-4 Boolean Analysis of Logic Circuits	199-203 203-205	2	E.g. 4-3 to 4-7 Problem: 9 to 18
12.	4-5 Logic Simplification Using Boolean Algebra 4-6 Standard Forms of Boolean Expressions	205-209 209-216	2	E.g. 4-9 to 4-12, 4-14 to 4-19 Problem: 19 to 30
13.	4-8 The Karnaugh Map 4-9 Karnaugh Map SOP Minimization	219-222 222-232	2	E.g. 4-23 to 4-32 Problem: 37 to 47
14.	**Multisim Lab 3**		**1**	E.g. 4-8, 4-13
15.	**Lab Assessment 1**		**1**	
	Chapter 5 Combinational Logic Analysis	261- 279	**6**	
16.	5-1 Basic Combinational Logic Circuits 5-2 Implementing Combinational Logic	262-267 267-272	3	E.g. 5-1 to 5-8 Problem: 1 to 19
17.	5-3 The Universal Property of NAND and NOR Gates 5-4 Combinational Logic Using NAND and NOR Gates	272-274 274-279	3	E.g. 5-9 to 5-11 Problem: 20 to 27
18.	**Multisim Lab 4**		**1**	E.g. 5-6
	Chapter 6 Functions of Combinational Logic	313-358	**10**	
19.	6-1 Half and Full Adders 6-2 Parallel Binary Adders	314-317 317-322	3	E.g. 6-1 to 6-4 Problem: 1 to 10
20.	6-4 Comparators	327- 331	1	E.g. 6-6, 6-7 Problem: 13 to 15
21.	6-5 Decoders 6-6 Encoders	331-338 341-343	3	E.g. 6-8 to 6-11 Problem: 16 to 24
22.	6-8 Multiplexers (Data Selectors) 6-9 Demultiplexers	347-356 356-358	3	E.g. 6-14 to 6-18 Problem: 28 to 31
23.	**Multisim Lab 5**		**1**	Simulation on half-adder

No.	Chapter	Page	Period	Detail Lecture Plan
				Simulation on comparator
24.	**Multisim Lab 6**		**1**	Simulation on encoder Simulation on 3-to-8 decoder
25.	**Lab Assessment 2**		**1**	
26.	All Chapters Revision		**2**	